Interfacing Spansion Flash to TI OMAP Processors

Application Note

Introduction

References

- S29GL-N MirrorBit™ Flash Family Data Sheet, Publication Number S29GL-N_00, Revision A, Amendment 7, Issue Date February 14, 2005.
- S29WS-N MirrorBit Flash Family Data Sheet, Publication Number S29WS-N_00, Rev G, Amendment 0, January 25, 2005.
- OMAP5912 Multimedia Processor Device Overview and Architecture Reference Guide (spru742.pdf).
- OMAP5912 Multimedia Processor Initialization Reference Guide (spru752B.pdf).
- OMAP5912 Multimedia Processor OMAP3.2 Subsystem Reference Guide (spru749A.pdf).

This application note assumes that the reader is familiar with asynchronous, page and synchronous flash memory timings.

The Texas Instruments OMAP 5912 processor is used as example in this application note. The OMAP 5912, 1510, 1610, 1710, 7xx, and 850 OMAP processors use the EMIF block (External Memory Interface) to provide the memory interface; therefore, this information is applicable to these, and most TI OMAP processors.

This application note describes the OMAP processor flash memory interface and the configuration registers that must be programmed to enable the different interface modes, including: configuring the processor and the flash device (if needed) for standard asynchronous operation, asynchronous page mode operation, and synchronous burst mode operation.

The OMAP traffic controller (TC) is the central interconnect that manages all accesses to external memories. The EMIF is divided into two distinct function blocks: EMIFS (External Memory Interface Slow), and EMIFF (External Memory Interface Fast). EMIFF provides an external 16-bit interface to SDRAM memories and is irrelevant to this application note. EMIFS is a 16-bit interface to ROM, flash and SRAM memories and is the subject of focus in this application note.

Additionally, the signals required to interface to the Spansion flash, the configuration required for the interface, the registers in both the OMAP processor and the flash that need to be programmed, and the interface timing are described.

Interface Signals

The OMAP 5910 provides four external chip-select signals that can be used to interface to flash devices: CS0, CS1, CS2, and CS3. Each external chip-select has an address range of 64 Mb, and supports asynchronous RAM, ROM, as well as asynchronous (page or standard) or synchronous burst flash. Each chip select can be independently configured via the software for logical 16 or 32 bit transfers although those transfers physically occur over an external 16-bit interface. For example, if configured for 32-bit transfers, each software request for a 32-bit transfer translates into two 16-bit transfers on the bus. Each chip-select has corresponding configuration registers to specify the protocol for the associated external device.

Table 1 describes the processor's flash signals.

Table I.   Flash Signals

Signal Name	I/O	Description
FLASH.RDY	I	Ready/busy signal from device. Used in synchronous burst mode only. After the initial access delay, the processor checks this signal on the rising edge of each clock cycle. If FLASH.RDY is high, data on the next clock rising edge is valid, and control signals such as chip select and output enable are extended another clock cycle.
FLASH.WP#	O	Flash write protect. This pin is controlled through an OMAP internal register, and can be used to drive the flash WP# pin, protecting specific sectors in the flash device.
FLASH.CLK	O	Clock signal for flash device for synchronous read accesses. Only active externally if the interface is configured for synchronous reads. FLASH.CLK = REF_CLK. REF_CLK is a factor of the system clock TC_CLK.
FLASH.RP#	O	Flash reset
FLASH.CSO#	O	Active-low chip-select
FLASH.CS1#	O	Active-low chip-select
FLASH.CS2#	O	Active-low chip-select for device. FLASH.BAA# and FLASH.CS2# are multiplexed on the same device pin. Pin function is selected using the configuration register, FUNC_MUX_CRTL_0. FLASH.CS2 functionality is set as the default. If FLASH.BAA# is used, one chip select is unavailable.
FLASH.CS3#	O	Active-low chip-select
FLASH.BAA#	O	Active-low burst advance acknowledge. FLASH.BAA# AND FLASH.CS2# are multiplexed on the same device pin. Pin function is selected using the configuration register, FUNC_MUX_CRTL_0. FLASH.CS2 functionality is set as the default. If FLASH.BAA# is used, one chip select is unavailable. Selecting the FLASH.BAA function disables the FLASH.CS2 functionality. Early flash burst devices required a BAA signal. The latest devices do not use this signal.
FLASH.OE#	O	Active-low output enable
FLASH.WE#	O	Active-low write enable
FLASH.ADV#	O	Active-low address valid. Present in both asynchronous and synchronous burst modes. Not always used by the flash device.
FLASH.D[15:0]	I/O	Flash data bus
FLASH.A[24:1]	O	Flash address bus
FLASH.BE#[1:0]	O	Active low external byte enables. Typically not required by flash devices.

Configuration Overview

Depending on the type of flash device used, the EMIFS interface must be initialized to maximize performance. In addition, if the flash device supports the synchronous burst interface, it must be initialized.

For a synchronous burst flash device, both EMIFS chip select configuration registers and the flash device must be configured. Other important factors to consider are:

■ read mode
■ clock frequency
■ data bus width
■ burst sequence (EMIFS only supports linear burst)
■ burst length
■ flash device highest clock rate
■ flash device initial access time

For both asynchronous and synchronous modes, all EMIFS control signals are referenced to an internal EMIFS reference clock (REF_CLK). The internal EMIFS reference clock is divided from the Traffic Controller (TC) clock by a programmable value in the FCLKDIV bit field of the EMIFS chip select configuration register (EMIFS_CSx_CONFIG). After reset or power up the EMIFS chip-selects default to asynchronous mode with 15 wait states and a clock divider of 6 relative to the traffic controller clock. This configuration defaults to a very long access time to ensure maximum compatibility with most external devices on power up.

In the synchronous mode, the active EMIFS clock is output on the FLASH.CLK pin. In asynchronous mode, the pin is driven inactive low, although the clock signal is still used as an internal reference to program the different control signals.

The OMAP processor only issues linear, incrementing, and fixed size 4 x 32Words access bursts (8 16-bit word bursts). Burst access is aligned on the burst size address boundary (starting burst LSB address A[3-0] is always equal to [0000]). This means the burst accesses are linear (or continuous) with no wrap around. External devices like synchronous flash memory require a burst protocol programming to conform to the EMIFS burst protocol.

Depending on the flash device and operating mode used, two main processor registers must be configured: the EMIFS Chip Select Configuration, and the Advanced EMIFS Chip Select Configuration Registers.

Table 2 shows the EMIFS Chip Select Configuration Register bit definition. There is one register for each chip select. This register defines the interface timing to the flash device.

Table 2.   EMIFS Chip Select Configuration Register (Sheet 1 of 2)

Bit	Field	Description
31	PGWSTEN	0: PGWST (Page mode wait states) is specified by bits 15:12. 1: PGWST (Page mode wait states) is specified by bits 30:27. Typically set to *1*. If not in page mode, this setting is disregarded by the processor.
30:27	PGWST	When in asynchronous page mode, (PGWST + 1) * REF_CLK specifies the access time for accesses within a page (the delay between successive words within the page or in-page wait states).

Table 2.   EMIFS Chip Select Configuration Register (Sheet 2 of 2)

Bit	Field	Description
26:23	BTWST	Controls the idle time in between processor cycles. Control signals are de-asserted during this time. Idle time is (BTWST +1) * TC_CK.
22	MAD	Enables EMIFS multiplexed address and data bus operation. 0: Non-multiplexed protocol 1: Multiplexed protocol
21	RESERVED	Must always be written to *0*.
20	BW	Controls the data bus width for this chip select. 0: 16-bit data bus. 1: 32-bit data bus.
19	RESERVED	Undefined read-only bit
18:16	RDMODE	The operation mode of the EMIFS for a given chip-select region is selected by the RDMODE bit field. Operations supported are: **Mode 0**. Standard asynchronous read. Used for any asynchronous memory, including flash devices. **Mode 1-2-3**. Asynchronous page mode read with 4 (mode 1), 8 (mode 2), or 16 (mode 3) words per page. These modes are used for page mode flash devices. **Mode 4-5**. Synchronous burst read (with burst advance control for mode 4). These modes are used for synchronous burst flash devices. **Mode 7**. Synchronous pipelined burst read. This mode is mainly used for TI embedded IC ROM and RAM memories. Note that all write accesses are asynchronous regardless of the operating mode selected by the RDMODE field.
15:12	PGWST/WELEN	Controls the number of wait states for accesses within a page for asynchronous page mode (PGWST). Also controls the WE pulse width (WELEN) during a write access. When PGWSTEN (bit 31) is *0*, this bit specifies both PGWST and WELEN. When PGWSTEN is *1*, this bit specifies only WELEN. PGWSTEN is typically set to *1*; therefore, this bit field typically specifies WELEN which is the WE pulse length during a write access. The page mode access time or the width of the WE# pulse is (WELEN + 1) * REF_CLK.
11:8	WRWST	The chip select and address setup time from WE low is (WRWST + 1) * REF_CLK. Only used for write accesses.
7:4	RDWST	Controls chip select pulse width for asynchronous read mode and the initial chip select pulse width for asynchronous read page mode and synchronous read mode. The chip select pulse width is defined as (RDWST + 2) * REF_CLK.
3	RESERVED	Reserved. Writing to this bit has no effect. Reading this bit returns an undefined value.
2	RT	Enable the read re-timed protocol. This bit may be *1* only in RDMODE 4, 5 and 7. The system will hang if the re-timing bit is set in other modes. 0: Non retimed protocol 1: re-timed protocol. Set to *0* for typical flash devices.
1:0	FCLKDIV	In all modes of operation, all EMIFS to memory control signals and timing are referenced to REF_CLK. Depending on the chip select configuration this internal clock can be available outside on the FLASH.CLK output pin. REF_CLK is divided from TC_CK (traffic controller clock) by the value contained in the FCLKDIV bit field. 00: REF_CLK = TC_CK divided by 1 01: REF_CLK = TC_CK divided by 2 10: REF_CLK = TC_CK divided by 4 11: REF_CLK = TC_CK divided by 6

The second OMAP register that must be programmed is the Advanced EMIFS Chip Select Configuration Register. Table 3 shows the Advanced EMIFS Chip Select Configuration Register bit definition.

Table 3.   Advanced EMIFS Chip Select Configuration Register

Bit	Field	Description
31:10	RESERVED	Reserved. Should be written to *0* and read value should be considered undefined.
9	BTMODE	Enables extended BTWST usage. 0: Bus turn around control and RD to RD/WR same as CS pulse width high control 1: Bus turn around control and RD/WR to RD/WR same as CS pulse width high control. If not set, some back-to-back accesses occur where the chip select signal is not deactivated. In general BTMODE should be set.
8	ADVHOLD	Controls the ADV pulse width low. ADV pulse width equals (ADVHOLD + 1) * REF_CLK. At a minimum, the ADV pulse width is equal to one REF_CLK cycle. If there is a need to extend ADV pulse width, ADVHOLD can be programmed to a non-zero value.
7:4	OEHOLD	Controls the time from OE high to CS high. (OEHOLD) * REF_CLK is the time from OE high to CS high. Note that because the CS minimum pulse width is 2 * REF_CLK, OESETUP must be set so (OESETUP + OEHOLD) is ≤ to RDWST. If this rule is violated, the processor produces a bad access completion. Refer to the OMAP5912 Reference Guide for more information.
3:0	OESETUP	Controls the time from CS low to OE low. Time from CS low to OE low is (OESETUP) * REF_CLK. Note that because the CS minimum pulse width is 2 * REF_CLK, OESETUP must be set so (OESETUP + OEHOLD) is ≤ to RDWST. If this rule is violated, the processor produces a bad access completion. Refer to the OMAP5912 Reference Guide for more information.

After power up in most systems, the flash device must be configured to avoid incorrect accesses. The following sections are provided as examples.

Asynchronous Read Operation Example

For this example, the S29GL256N with 110-ns asynchronous access time, an OMAP5912, and a basic system clock of 100 MHz are used. The S29GL256N does not need to be configured. In the OMAP processor, FCLKDIV is configured to 00 so that REF_CLK = TC_CK = 10 ns. REF_CLK is the basic unit of measure for setting timing parameters in the OMAP processor. Asynchronous read mode is selected by programming the RDMODE bit field to 000 in the corresponding EMIFS chip-select configuration register. This is the default mode at reset.

Table 4 and Table 5 show the bit settings required for each of the register bits based on the S29GL256N specification. Refer to the S29GL256N data sheet for full specifications. First let's go through the EMIFS Chip Select Configuration Register bits.

Table 4.   EMIFS Chip Select Configuration Register, Bit Settings-Asynchronous

Bit	Field	Description
31	PGWSTEN	Set to *1*. PGWST (Page mode wait states) is specified by bits 30:27. Not important in this example since this is not page mode. Typically set to *1*. If not in page mode, this setting is disregarded by the processor.
30:27	PGWST	Set to 000. Not important in this example since this is not page mode.
26:23	BTWST	Controls the idle time in between processor cycles. Idle time is (BTWST +1) * TC_CK. Set to 0011 for this example. This allows for four TC_CK clock cycles (40 ns total) of idle time in between asynchronous flash accesses. The S29GL256N requires a minimum of 35 ns from the end of a write cycle to the beginning of a read cycle.
22	MAD	Set to *0* for Non-multiplexed operation.
21	RESERVED	Set to *0*. Must always be written to *0*.
20	BW	Controls the data bus width for this chip select. Set to *0* since S29GL256N has a x16 bit bus.
19	RESERVED	This is a don't care, read only bit that is undefined.
18:16	RDMODE	Set to 000, standard asynchronous read. Note that all write accesses are asynchronous regardless of the operation mode selected by the RDMODE field.
15:12	PGWST/WELEN	Since bit 31 is *0*, these bits control the WE pulse width during a write access. The minimum WP# pulse width for S29GL256N is 35ns. The width of the WE# pulse is (WELEN + 1) * REF_CLK. Setting WELEN to 0101 configures the WE# pulse for 60 ns. This allows more than the 45 ns of data setup to WE# going high that the S29GL256N requires.
11:8	WRWST	The chip select and address setup time from WE low is (WRWST + 1) * REF_CLK. Chip select and address setup required is *0* ns minimum. Setting WRWST to 0000 provides 10 ns of chip select and address setup time.
7:4	RDWST	Controls chip select pulse width for asynchronous read mode and the initial chip select pulse width for asynchronous read page mode, and synchronous read mode. The chip select pulse width is determined by (RDWST + 2) * REF_CLK. Since this example uses a 110-ns S29GL256N, chip enable must be held low for at least 110 ns to guarantee data out from the flash. Setting the chip select pulse width to 1010 configures the chip for 120 ns.
3	RESERVED	Reserved. Writing to this bit has no effect. Reading it returns an undefined value.
2	RT	Enables the read re-timed protocol. This bit may be *1* only in RDMODE 4, 5 and 7 only; therefore, set it to *0*.
1:0	FCLKDIV	In all modes of operation, all EMIFS to memory control signals and timing are referenced to REF_CLK. 00: REF_CLK = TC_CK divided by 1 01: REF_CLK = TC_CK divided by 2 10: REF_CLK = TC_CK divided by 4 11: REF_CLK = TC_CK divided by 6 Setting FCLKDIV to 00 makes REF_CLK = TC_CK = 100 MHz. This results in a 10-ns unit of time, of which all parameters in this table are a factor.

Table 5 describes the Advanced EMIFS Chip Select Configuration Register bits.

Table 5.   Advanced EMIFS Chip Select Configuration Register, Bit Settings

Bit	Field	Description
31:10	RESERVED	Reserved. Should be written to *0* and read value should be considered undefined.
9	BTMODE	Enables extended BTWST usage. 0: Bus turn around control and RD to RD/WR same CS pulse width high control 1: Bus turn around control and RD/WR to RD/WR same CS pulse width high control. BTMODE *0* implies that in some cases, for instance, burst write accesses, the chip select signal is not activated. In this example BTMODE is configured to *1* for safest operation, and to make sure that the chip select signal is deactivated between accesses.
8	ADVHOLD	Controls the ADV pulse width low. ADV pulse width equals (ADVHOLD + 1) * REF_CLK. Although not used by the S29GL256N device, ADVHOLD must be programmed because ADV signal timing is used to generate other signals in the OMAP processor. ADVHOLD is programmed to *1*, which produces an ADV signal that is 20-ns low duration.
7:4	OEHOLD	Controls the time from OE high to CS high. (OEHOLD) * REF_CLK is the time from OE high to CS high. Note that because CS minimum pulse width is 2 * REF_CLK, OESETUP must be set so that (OESETUP + OEHOLD) is ≤ RDWST. If this rule is violated the processor produces a bad access completion. Refer to the OMAP5912 Reference Guide for more information. For this example, OEHOLD is set to 0001. OE signal goes high 10 ns before the chip select signal goes high.
3:0	OESETUP	Controls the time from CS low to OE low. Time from CS low to OE low is (OESETUP) * REF_CLK. Note that because the CS minimum pulse width is 2 * REF_CLK, OESETUP must be set so that (OESETUP + OEHOLD) is ≤ RDWST. If this rule is violated the processor produces a bad access completion. Refer to the OMAP5912 Reference Guide for more information. OESETUP is set to 0001 resulting in 10 ns from CS low to OE low.

Since there are no registers to configure in the S29GL256N, this completes the asynchronous read mode operation example.

Asynchronous Page Mode Read Operation Example

The asynchronous page mode read operation is similar to the asynchronous read. The only difference is that the number of wait states (REF_CLK clock cycles) is different between the first access within a page and subsequent accesses within the page. This example uses the S29GL256N, which has an initial access time of 110 ns and a page access time of 30 ns. The page size is 8 words.

The S29GL256N does not require any configuration. For the OMAP processor, most of the configuration values used in the previous asynchronous example remain valid. Changes are needed for the read mode configuration and the in-page access parameters.

The following parameters are changed:

■ RDMODE, selects the type of memory access and number of words per page for page mode devices. Mode 2 (010) supports page mode accesses for flash devices with 8 words. Set RDMODE = 010.

■ RDWST sets the delay to insert prior to latching the first data word read from a page (range 0-7). This is the initial access time for the device, which is also 110 ns. This parameter does not change from the previous standard asynchronous example, and is set to 120 ns. When crossing a page boundary, the RDWST parameter is used again for the first access on the new page. Set RDWST = 1010.

■ PGWST is important in this example. PGWST defines the in-page wait states to be used; it sets the delay between subsequent words in the page (range 0-7). The resulting delay is equal to (PGWST+1) * REF_CLK. The S29GL256N device has a 30-ns page access time. With REF_CLK = 10 ns, PGWST = 0011 sets the in-page wait state to 40 ns.

This completes this example. The device is configured for an initial access of 120 ns with in-page accesses of 40 ns.

Synchronous Burst Read Operation Example

This example uses the S29WS256N synchronous burst flash device. Refer to the S29WS256N data sheet for full specifications (Publication Number S29WS-N_00_G0). For demonstration purposes, the 54-MHz version of this device is used. The main device parameters are:

■ maximum synchronous initial latency (t_{IACC}) = 80 ns; this is the initial synchronous access time

■ maximum synchronous burst access (t_{BACC}) = 13.5 ns; This is the clock-to-clock access time of the device after a burst cycle has started.

■ maximum asynchronous address and CE# access t_{ACC} = t_{CE} = 80 ns. This is important because all writes are asynchronous accesses to the device.

■ general setup and hold times are also important and should be met as well.

On power up, the S29WS256N defaults to standard asynchronous mode. To operate in synchronous burst mode, both the flash device and the processor, in this order, must be configured for synchronous burst mode of operation.

The basic processor clock in these examples has been 100 MHz (TC_CLK = 10 ns). In synchronous burst mode the REF_CLK clock signal of the OMAP processor appears externally on the FLASH.CLK signal output. FLASH.CLK is directly connected to the flash clock signal. Once a burst cycle has started, data is read from the flash device on every single rising edge of FLASH.CLK. Therefore FLASH.CLK can not exceed the maximum operating frequency of the S29WS256N device. Since 54 MHz is the maximum frequency of the S29WS256N device in this example, TC_CLK is divided by 2 to provide a 50 MHz clock to the flash (FLASH.CLK = REF_CLK = TC_CLK / 2 = 20-ns period.). Since the maximum initial synchronous latency (t_{IACC}) of the flash device is 80 ns, 5 REF_CLK clock cycles (100 ns) for initial data access are used. Using less than 5 clock cycles leaves no margins to account for system delays and required setup/hold times. On the last FLASH.CLK rising edge of the initial access period (the 5th rising edge in this example), the OMAP processor samples the FLASH.RDY signal provided by the flash device. If FLASH.RDY is asserted then the data on the next FLASH.CLK rising edge is assumed to be valid. If FLASH.RDY is not asserted then data is assumed not to be valid on the next rising edge and the processor waits or extends the access until FLASH.RDY is asserted. This process continues on every clock cycle until the processor aborts the burst cycle. This method for interpreting the FLASH.RDY signal is referred to as *ready asserted one clock cycle before data*.

Once configured for synchronous burst mode, the OMAP processor only issues linear, incrementing, and fixed size 8-word access bursts. In addition, burst accesses are always aligned on burst size address boundary (starting burst LSB address A[0-3] is always equal to [0000]).

Table 6 describes the flash device configuration register bit fields that must be programmed to work with the OMAP processor.

Table 6.   S29WS256N Configuration Register, Bit Settings

Bit	Function	Description
CR15	Device Read Mode	Set to *0* for synchronous burst operation.
CR14	Boundary Crossing	Set to *0* for no extra boundary crossing latency. Must be set to *1* for frequencies above 54 MHz as dictated by the flash data sheet.
CR[13:11]	Programmable Wait States	Set to *011*, data valid on the 5th active clock edge after addresses latched. Note that FLASH.CLK = 20 ns. Since the maximum initial synchronous latency (t_{IACC}) of the flash device is 80 ns, 5 REF_CLK clock cycles (100 ns) are used for initial data access. Using less than 5 clock cycles leaves no margins to account for system delays and required setup/hold times.
CR10	RDY output pin polarity	Set to *1* for RDY signal active high. FLASH.RDY input to the OMAP processor is asserted high.
CR9	RESERVED	Set to *1*. Default
CR8	RDY	Set to *0*. RDY active one clock cycle before data is valid. The OMAP processor monitors the RDY signal on the rising edge of each clock cycle. If RDY is high then it assumes data is valid on the next rising edge.
CR[7:4]	RESERVED	Read or write to *1100*.
CR3	Burst Wrap Around	Set to *0* for no wrap around burst. The OMAP processor only issues linear, incrementing, and fixed size 8-word access bursts. In addition, burst accesses are always aligned on burst size address boundary (starting burst LSB address A[0-3] is always equal to [*0000*]).
CR[2:0]	Burst Length	Set to *000* for continuous burst. The OMAP processor does not know how to handle wrap around of the burst data. The OMAP processor only issues linear, incrementing, and fixed size 8-word access bursts. In addition, burst accesses are always aligned on burst size address boundary (starting burst LSB address A[0-3] is always equal to [*0000*]). The recommended setting is for continuous burst.

Table 7 describes each of the bit fields that must be programmed in the OMAP processor. Identical to previous examples, the appropriate Chip Select EMIFS Configuration Register must be programmed.

Table 7.   EMIFS Chip Select Configuration Register, Bit Settings for Burst (Sheet 1 of 3)

Bit	Field	Description
31	PGWSTEN	Set to *1*. If not in page mode, this setting is disregarded by the processor. PGWST (Page mode wait states) is specified by bits 30:27.
30:27	PGWST	In synchronous burst, this field has no effect. Set PGWST = *0000*
26:23	BTWST	Controls the idle time between processor cycles. Idle time is (BTWST +1) * TC_CK. Set BTWST to *0011*. This allows 40 ns of idle time between back-to-back cycles.
22	MAD	Set MAD = *0* for non-multiplexed protocol.
21	RESERVED	Must always be written to *0*.
20	BW	Set BW = *0* for 16-bit data bus.
19	RESERVED	Undefined read only bit.

Table 7.   EMIFS Chip Select Configuration Register, Bit Settings for Burst (Sheet 2 of 3)

Bit	Field	Description
18:16	RDMODE	Set RDMODE = *100* for mode 4. The operation mode of the EMIFS for a given chip-select region is selected by the RDMODE bit field. Operations supported are: — Mode 0. Standard asynchronous read. Used for any asynchronous memory, including flash devices. — Mode 1-3. Asynchronous page mode read with 4 (mode1), 8 (mode 2), or 16 (mode 3) words per page. These modes are used for page mode flash devices. — Mode 4-5. Synchronous burst read (with burst advance control for mode 4). These modes are used for synchronous burst flash devices. — Mode 7. Synchronous pipelined burst read. This mode is mainly used for TI embedded IC ROM and RAM memories. Note that all write accesses are asynchronous regardless of the operation mode selected by the RDMODE field. For this example, either mode 4 or mode 5 can be used. Both of these modes work with the S29WS256N device. Set RDMODE = *100* for mode 4.
15:12	PGWST/WELEN	Controls the number of wait states for accesses within a page for asynchronous page mode. Also controls the WE pulse width during a write access. When PGWSTEN (bit 31) is *0*, this bit specifies both PGWST and WELEN. When PGWSTEN is *1*, this bit specifies only WELEN. PGWSTEN is typically set to *1*; therefore, this bit field specifies WELEN, which is the WE pulse length during a write access. The minimum WE pulse width needed by the S29WS256N is 30 ns. The width of the WE# pulse is (WELEN + 1) * REF_CLK. Setting WELEN = *0010* generates a 60-ns WE# pulse width. Note that all write cycles are always asynchronous cycles.
11:8	WRWST	The chip select and address setup time from WE low is (WRWST + 1) * REF_CLK. Setting WRWST = *0000* will provide a 20-ns chip select and address setup time from WE# low.
7:4	RDWST	Set RDWST = *0100*. In synchronous read modes RDWST controls the initial chip select pulse width. The initial chip select pulse width is determined by (RDWST + 2) * REF_CLK. The first access is completed when both the internal RDWST wait state expires and FLASH.RDY is asserted by the external device. The flash device was configured for data valid on the 5th active clock edge after addresses latched. The clock cycle where addresses are latched must also be counted for RDWST; therefore, the total initial pulse width for chip select is 6 REF_CLK clock cycles. Set RDWST = *0100*. At the 6th active clock edge the processor checks FLASH.RDY signal to determine whether or not the data is valid on the next clock cycle. If FLASH.RDY is not asserted, the processor adds a one clock cycle wait state. This is repeated every clock cycle until the processor completes the burst cycle.
3	RESERVED	Reserved. Writing to this bit has no effect. Reading it returns an undefined value.

Table 7.   EMIFS Chip Select Configuration Register, Bit Settings for Burst (Sheet 3 of 3)

Bit	Field	Description
2	RT	Set RT = *0*. This bit enables the read re-timed protocol. This bit may be *1* only in RDMODE 4, 5 and 7 only. The system hangs if the re-timing bit is set in other modes. 0: Non retimed protocol. 1: retimed protocol. To work with S29WS256N, set RT = *0*.
1:0	FCLKDIV	Set FCLKDIV = *01*. In all modes of operation, all EMIFS to memory control signals and timing are referenced to REF_CLK. In synchronous burst modes this internal clock appears outside on the FLASH.CLK output pin. REF_CLK is divided from TC_CK (traffic controller clock) by the value contained in the FCLKDIV bit field. 00: REF_CLK = TC_CK divided by 1 01: REF_CLK = TC_CK divided by 2 10: REF_CLK = TC_CK divided by 4 11: REF_CLK = TC_CK divided by 6 Using a clock of 100 MHz (TC_CK) and on a 54-MHz maximum frequency S29WS256N flash device, divide TC_CK by 2 to provide a 50-MHz clock on the FLASH.CLK output. Set FCLKDIV = *01*.

Table 8 describes the Advanced EMIFS Chip Select Configuration Register bits.

Table 8.   Advanced EMIFS Chip Select Configuration Register, Bit Settings (Sheet 1 of 2)

Bit	Field	Description
31:10	RESERVED	Reserved. It is recommended that this bit be written to *0* and read value be considered undefined.
9	BTMODE	Set BTMODE = *1*. Enables extended BTWST usage. 0: Bus turn around control and RD to RD/WR same CS pulse width high control 1: Bus turn around control and RD/WR to RD/WR same CS pulse width high control. BTMODE *0* implies that in some cases the chip select signal is not de-activated between back-to-back cycles. In this example, BTMODE is configured to *1* for the safest operation and to make sure that the chip select signal is de-activated between accesses.
8	ADVHOLD	Set ADVHOLD = *1* to generate an ADV pulse that is two FLASH.CLK cycles long. ADVHOLD controls the ADV pulse width low. ADV pulse width equals (ADVHOLD + 1) * REF_CLK. In synchronous mode, the FLASH.ADV, FLASH.CS# and address signals are driven one REF_CLK cycle before the first FLASH.CLK rising edge is provided externally. This ensures that the chip select, ADV, and address valid setup time to the device clock rising edge is met. In case this is not enough to meet setup time requirements, ADVHOLD can be programmed to extend the FLASH.ADV pulse. In this example ADVHOLD is set to *1* to extend it one clock cycle.

Table 8.   Advanced EMIFS Chip Select Configuration Register, Bit Settings (Sheet 2 of 2)

Bit	Field	Description
7:4	OEHOLD	OEHOLD is a don't care in the synchronous modes, because FLASH.OE follows FLASH.CS signal as they are extended by the FLASH.RDY signal.
3:0	OESETUP	Set OESETUP = *0000*. OESETUP controls the time from CS low to OE low (OESETUP * REF_CLK). OESETUP on the S29WS256N can be set to either *0000* or *0001* with no difference in performance. Setting OESETUP = *0000*, brings FLASH.OE low at the same time as FLASH.CS.

This completes the synchronous burst example. The device is configured for an initial synchronous access of 100 ns (data 5 clock cycles after addresses latched) with in-burst accesses every 20 ns (50 MHz FLASH.CLK clock) and FLASH.RDY signal active one clock before data.

Revision Summary

Revision A (July 5, 2005)

Initial release.